

Abstract of the Disclosure

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A semiconductor package includes a semiconductor chip, a die pad, an adhesive, metal wires, LOC inner leads, and standard inner leads sealed within a sealing resin. The LOC inner leads and the standard inner leads are arranged in the same plane and both are arranged along one side of the semiconductor chip. Clearance between the inner leads and the die pad larger than the total thickness of the semiconductor chip and the bonding material. Thus, a semiconductor chip having electrode pads broadly distributed can be employed and the section modulus of the semiconductor package can be increased.